Integrated Device Technology, Inc.

1 MEGABIT (1024K x 1-BIT) CMOS STATIC RAM SIP MODULE

PRELIMINARY
IDT 7MC4001

FEATURES:

- High-density 1 megabit (1024K x 1) CMOS static RAM module
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 30-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 35ns (max.)
- Separate I/O lines
- Low power consumption
  - Dynamic: 1.35W (max.)
  - Full standby: 330mW (max.)
- Single 5V(±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

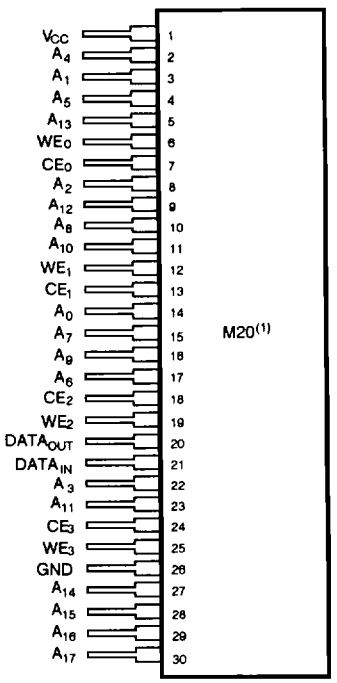
The IDT7MC4001 is a 1 megabit (1024K x 1-bit) high-speed static RAM module with separate I/O. The module is constructed on a co-fired ceramic substrate using four IDT71257 256K x 1 static RAMs in surface mount packages.

The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC4001 is offered in a 30-pin ceramic SIP (single in-line package). At only 420 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing five IDT7MC4001 modules to be stacked per inch of board space.

The IDT7MC4001 is available with maximum access times as fast as 35ns, with maximum power consumption of 1.35 watts. The module also offers a full standby mode of 330mW (max.).

All inputs and outputs of the IDT7MC4001 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

PIN CONFIGURATION

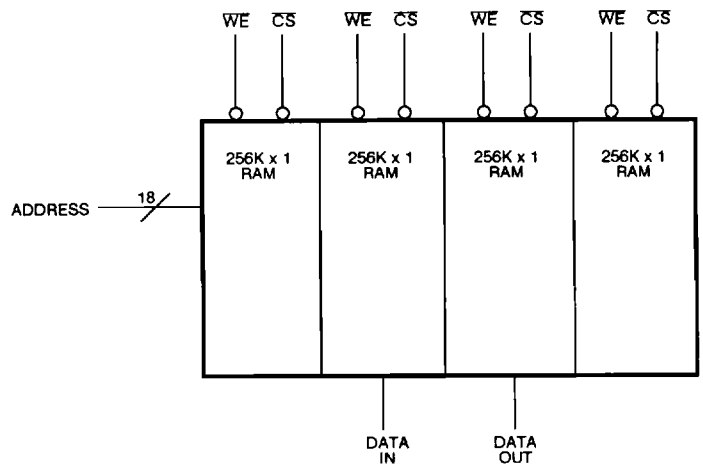


SIP
SIDE VIEW

NOTE:

1. For module dimensions, please refer to module drawing M20 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-17}	Address
$DATA_{IN}$	Data Input
$DATA_{OUT}$	Data Output
$\overline{CS}_{0-3}$	Chip Select
$\overline{WE}_{0-3}$	Write Enable
V_{CC}	Power
GND	Ground

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MC4001 MIN.	IDT7MC4001 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	50	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0	–	225	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}	–	245	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max., Output Open	–	180	mA
I_{SB1}	Full Standby Power Supply Current	CS ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CS} = Max., Output Open	–	60	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	V

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

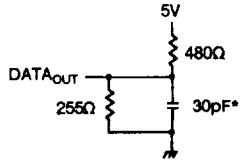


Figure 1. Output Load

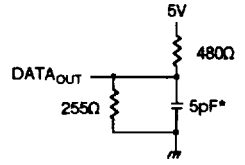


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MC4001S35 MIN.	MAX.	IDT7MC4001S45 MIN.	MAX.	IDT7MC4001S55 MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	10	–	10	–	10	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	25	–	35	–	45	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	35	–	45	–	55	ns

NOTE:
1. This parameter guaranteed but not tested.

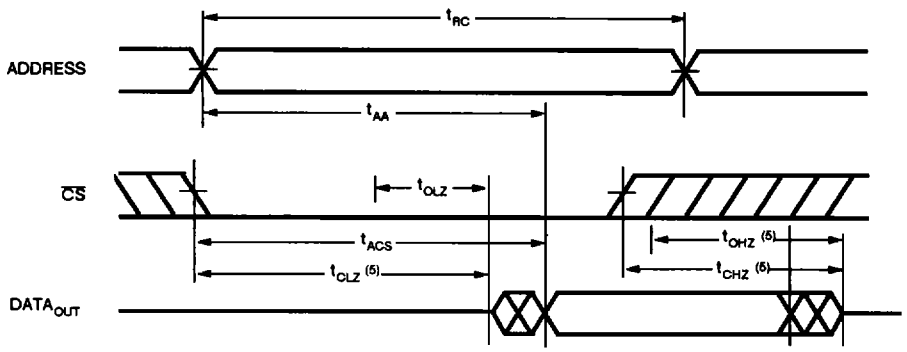
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

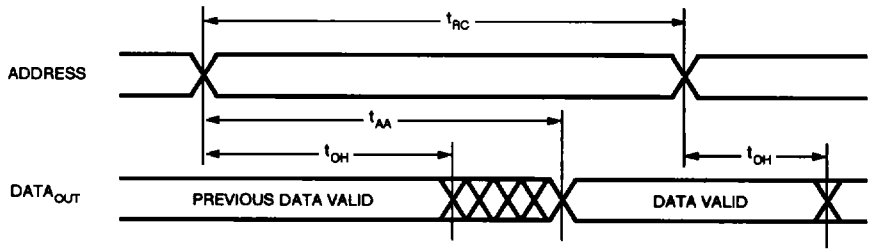
SYMBOL	PARAMETER	IDT7MC4001S35 MIN.	MAX.	IDT7MC4001S45 MIN.	MAX.	IDT7MC4001S55 MIN.	MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	25	–	30	–	40	ns
t_{DW}	Data Valid to End of Write	20	–	25	–	35	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

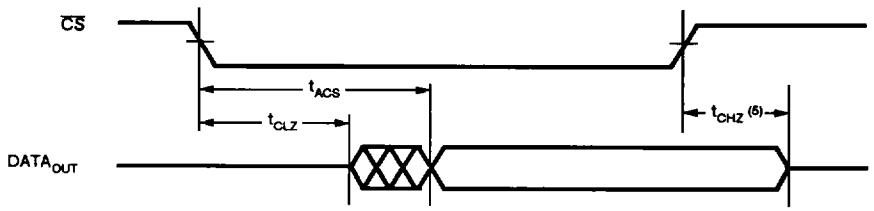
TIMING WAVEFORM OF READ CYCLE NO. 1 [1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3, 4]



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

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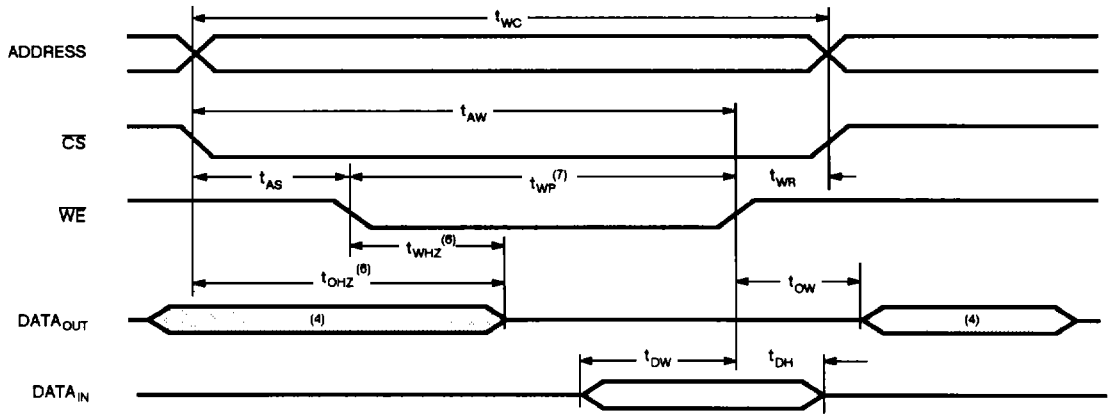
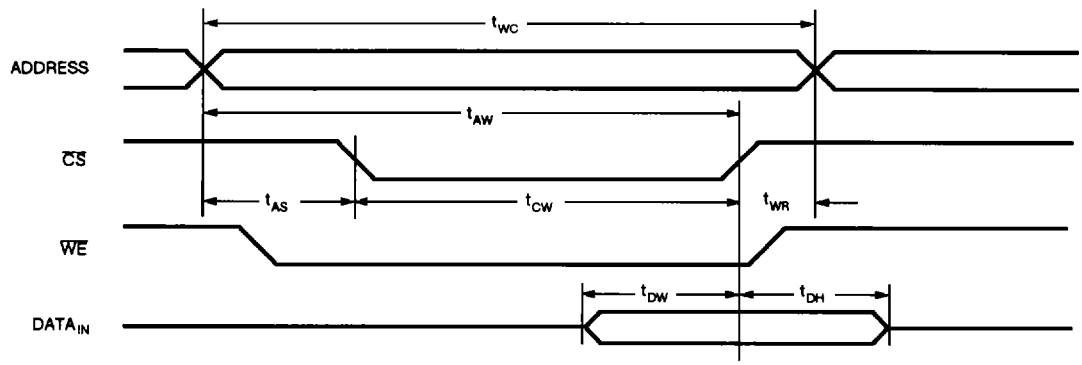
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

TRUTH TABLE

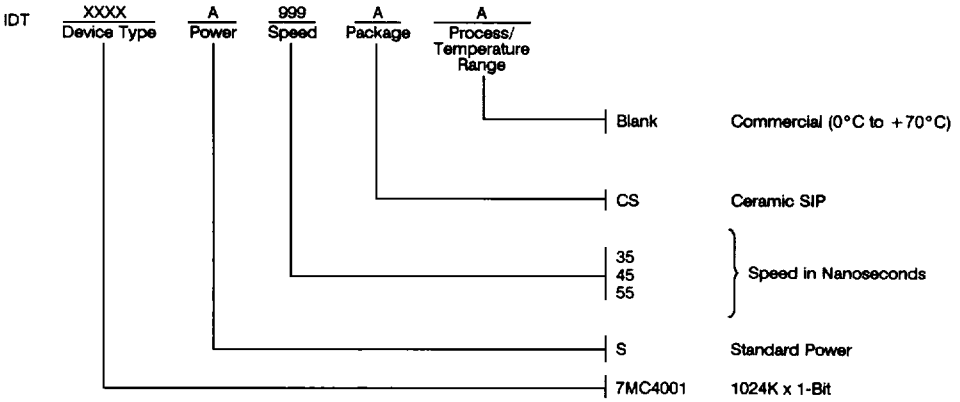
MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



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